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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,475	02/19/2002	Spencer Gold	SMQ-089/P6550	6691

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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,475	GOLD ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-13,16,17,21,22 and 26-38* is/are rejected.

7)☒ Claim(s) *7,8,14,15,19,20 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Upon further consideration, the allowable subject matter of claims 21, 22, 26 and 27 as indicated in the last Office Action mailed on October 3, 2003 has been withdrawn and replaced by the following office action. Any inconvenience to the Applicant(s) is regretted.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 21, 22, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. Pat. No. 6542846) in view of Gunther et al. (U.S. Pub. No. 2001/0021217) and Piosenka et al. (U.S. Pat. No. 5406630).

Miller et al. teach a controller for monitoring a temperature of an integrated circuit (see Abstract), comprising: a first interface for receiving a first value representative of a temperature of said integrated circuit, the first value is produced by one of an active thermal sensor and a passive thermal sensor formed in said integrated circuit (col. 4, lines 1-28 and col.4, lines 37-51); a second interface for receiving a second value

representative of a threshold temperature (col.9, lines 9 and col. 10, lines 1-4); and a comparator for comparing said first value to said second value (Fig. 5 and col.9, lines 9 and col. 10, lines 1-4).

Miller et al. do not mention: said first value is produced by an active thermal sensor formed in said integrated circuit; a comparator response logic coupled to said comparator for determining in response to a comparison of said first value to said second value by said comparator whether an over-temperature condition in said integrated circuit exists; said comparator response logic uses digital filtering to filter said first value representative of a temperature of said integrated circuit; a response buffer coupled to said comparator response logic for storing a value representative of a response to said over temperature condition; said controller comprises a microprocessor; and an interface from said comparator response logic to said microprocessor to enable said microprocessor to communicate with said comparator response logic.

Gunther et al. teach an integrated on-chip thermal management system, wherein an active thermal sensor formed in an integrated circuit is used to sense the temperature of said integrated circuit (sections 0027-0029). Gunther et al. further teach the step and means of digital filtering to filter said first value representative of a temperature of said integrated circuit (sections 0035-0038 and 0050).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Gunther et al. in the system of Miller et al.

in order to actively monitor the die temperature across said integrated circuit (Gunther et al., section 0029).

Piosenka et al. teach a comparator response logic coupled to comparators for determining in response to a comparison of a first value to a second value by said comparators whether an over-temperature condition in an integrated circuit exists (col. 6, lines 9-54). Piosenka et al. further teach: a response buffer coupled to said comparator response logic for storing a value representative of a response to said over temperature condition (col. 5, lines 17-31); a microprocessor; and an interface from said comparator response logic to said microprocessor to enable said microprocessor to communicate with said comparator response logic (col. 6, lines 55-61).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Piosenka et al. in the combination of Miller et al. and Gunther et al. in order to provide a low-cost and efficient mechanism for judging the existence of an over-temperature condition in an integrated circuit (Piosenka et al., col. 6, lines 25-54).

4. Claims 2-5, 9, 11, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. Pat. No. 6542846) in view of Gunther et al. and Piosenka et al., as applied to claim 1 above, and further in view of McMinn (U.S. Pat. No. 6098030).

Miller et a., Gunther et al. and Piosenka et al. teach a system and method that includes the subject matter discussed above. Gunther et al. further teach: a serial temperature capture device for receiving a plurality of temperatures of said integrated

circuit, wherein said serial temperature capture device is adapted to receive a plurality of temperatures from a plurality of thermal sensors (sections 0033, 0051 and 0052).

Miller et al., Gunther et al. and Piosenka et al. do not state explicitly that: said controller further comprises a temperature measurement buffer for holding said first value received from said first interface; sequentially providing said plurality of temperatures of said integrated circuit to said temperature measurement buffer; a threshold buffer corresponding to said temperature measurement buffer and adapted to store a second value representative of a threshold temperature; a microprocessor adapted to communicate with said temperature measurement buffer to read said first value and thermally profile said integrated circuit; a plurality of temperature measurement buffers, wherein each temperature measurement buffer is adapted to receive a value representative of a temperature of an integrated circuit; a serial temperature capture device for receiving a plurality of temperatures of said integrated circuit and providing said plurality of temperatures of said integrated circuit to said plurality of temperature measurement buffers.

McMinn discloses a thermal management system for an operating integrated circuit (see Abstract), and teaches a controller comprising: a temperature measurement buffer for holding said first value received from said first interface (col. 4, lines 47-54; col. 5, lines 41-56 and col. 6, lines 47-67); a threshold buffer corresponding to said temperature measurement buffer and adapted to store a second value representative of a threshold temperature (col. 4, lines 47-54 and col. 7, lines 37-44); a microprocessor adapted to communicate with said temperature measurement buffer to read said first

value and thermally profile said integrated circuit (col. 3, lines 1-7, lines 25-30; and col. 4, lines 35-46); a serial temperature capture device for receiving a plurality of temperatures of said integrated circuit and sequentially providing said plurality of temperatures of said integrated circuit to said temperature measurement buffer (col. 4, line 55 to col. 5, line 23); a plurality of temperature measurement buffers, wherein each temperature measurement buffer is adapted to receive a value representative of a temperature of an integrated circuit (Figs. 1-3; col. 4, line 55 to col. 5, line 23); a serial temperature capture device for receiving a plurality of temperatures of said integrated circuit and providing said plurality of temperatures of said integrated circuit to said plurality of temperature measurement buffers (Figs. 1-3; col. 4, line 55 to col. 5, line 23).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of McMinn in the combination of Miller et al., Gunther et al. and Piosenka et al. in order to provide a control circuit to thermally profile said integrated circuit in which both said temperature measurements and said threshold temperatures are programmable (McMinn, col. 3, lines 1-46).

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Gunther et al. and Piosenka et al., and further in view of McMinn, as applied to claims 1 and 11 above, and further in view of Pricer et al. (U.S. Pat. No. 5873053).

Miller et al., Gunther et al., Piosenka et al. and McMinn teach a system that includes the subject matter discussed above. The combination of Miller et al., Gunther et al., Piosenka et al. and McMinn do not mention explicitly that: a plurality of threshold

buffers corresponding to said plurality of temperature measurement buffers and adapted to store a plurality of second values representative of threshold temperatures.

Pricer et al. teach on-chip temperature sensors for control of chip operating temperature, wherein said sensors are capable of detecting undesirable temperature condition at different portion of said chip (col. 8, lines 7-26), and a threshold value is determined for each of said thermal sensor based on a location of said thermal sensor in said chip (col. 10, lines 27-38 and col. 11, lines 14-31).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Pricer et al. in the combination of Miller et al., Gunther et al., Piosenka et al. and McMinn to have a plurality of McMinn threshold buffers for storing a plurality of threshold temperatures, in order to provide a thermal management system which can detect any undesirable temperature condition at different portion of the integrated circuit (Pricer et al., Abstract; col. 8, lines 18-26 and col. 10, lines 27-38).

6. Claims 6, 10, 12 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Gunther et al. and Piosenka et al., and further in view of McMinn as applied to claims 1-5 and 11 above, and further in view of Senyk (U.S. Pat. No. 6363490) and Ristic et al. (U.S. Pat. No. 5291607).

Miller et al., Gunther et al., Piosenka et al. and McMinn teach a system and method that includes the subject matter discussed above. The combination of Miller et al., Gunther et al., Piosenka et al. and McMinn do not mention explicitly that: said threshold buffer is located external to said controller; at least one of said plurality of

temperature measurement buffers is located external to said controller; an interface from said first interface to a microprocessor to enable said microprocessor to read said first interface.

Senyk discloses a method and apparatus for monitoring the temperature of a processor, and teaches a controller that compares the temperature of the processor to a threshold, wherein said threshold is set by a buffer located external to said controller (col. 4, lines 32-42). Senyk further teaches that: a temperature sensing diode is located external to said controller.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Senyk threshold buffer in the combination of Miller et al., Gunther et al., Piosenka et al. and McMinn in order to separate the controller from the sensed environment so that the performance of the controller is not affected by any undesirable temperature condition of the sensed environment (Ristic et al., col. 1, lines 31-67).

It would also have been obvious to one having ordinary skill in the art at the time the invention was made to apply the teaching of Senyk arrangement for thermal sensor and controller to the combination of Miller et al., Gunther et al., Piosenka et al. and McMinn such that at least one of said temperature measurement buffers taught by McMinn is located external to said controller, in order to separate the controller from the thermal sensors so that the performance of the controller is not affected by any undesirable temperature condition of the sensed environment (Ristic et al., col. 1, lines 31-67).

Ristic et al. teach an interface to a microprocessor to enable said microprocessor to read output signals from a plurality of sensor cells (Fig. 1; col. 3, lines 21-32, lines 40-50 and col. 4, lines 50-63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the teaching of Ristic et al. to the Miller et al. processor in order to utilize said microprocessor to process data generated by said sensor cells (Ristic et al., col. 31-67).

7. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Gunther et al. and Piosenka et al., as applied to claim 1 above, and further in view of Pippin (U.S. Pat. No. 5838578).

Miller et al., Gunther et al. and Piosenka et al. teach a system and method that includes the subject matter discussed above. The combination of Miller et al., Gunther et al. and Piosenka et al. do not mention explicitly that: said controller further comprises an interface from said second interface to a microprocessor to enable said microprocessor to write to said second interface.

Pippin discloses a method and apparatus for programmable thermal sensor for an integrated circuit, and teaches a controller that comprises an interface to a microprocessor to enable said microprocessor to reset a threshold temperature (Fig. 9; and col. 13, lines 51-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Pippin in the combination of Miller et al.,

Gunther et al. and Piosenka et al. system in order to reset dynamically the threshold temperature for thermal management of said integrated circuit (Pippin, Abstract).

8. Claims 30, 31 and 35, 36, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. Pat. No. 6542846) in view of Piosenka et al. (U.S. Pat. No. 5406630).

Miller et al. teach a controller and method for monitoring a temperature of an integrated circuit (see Abstract), comprising the steps and means of: receiving a plurality of first values representative of a temperature of said integrated circuit (col. 4, lines 1-28 and col.4, lines 37-51); comparing said plurality of first values to a plurality of corresponding second values representative of a plurality of threshold temperatures (col.9, lines 9 and col. 10, lines 1-4); determining whether an over-temperature condition of said integrated circuit exists based on an output of said means and step for comparing (Fig. 5 and col.9, lines 9 and col. 10, lines 1-4). Miller et al. further teach: steps and means for determining a response to said over-temperature condition (col. 10, lines 5-30) and executing said response to said over-temperature condition (col. 10, lines 5-30).

Miller et al. do not mention monitoring die temperatures of an integrated circuit.

Piosenka et al. teach an apparatus for monitoring die temperatures of an integrated circuit (cols. 4-5, lines 25-31).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Piosenka et al. in the invention of Miller

et al. in order to monitor and control die temperature of a given integrated circuit (Piosenka et al., cols. 4-5, lines 25-31).

9. Claims 32 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Piosenka et al., as applied to claims 30, 31, 36 and 35 above, and further in view of Gunther et al.;

Miller et al. and Piosenka et al. teach an apparatus and method that includes the subject matter discussed above. Miller et al. and Piosenka et al. do not mention explicitly that: digitally filtering said output of said means for comparing before determining whether an over-temperature condition of said integrated circuit exists.

Gunther et al. teach the step and means of digitally filtering the output of a thermal sensor before determining whether an over-temperature condition of an integrated circuit exists (sections 0035-0038 and 0050).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Gunther et al. in the combination of Miller et al. and Piosenka et al. in order to dampen out or remove spurious signals (Gunther et al., section 0036).

10. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Piosenka et al., as applied to claims 30 above, and further in view of Ristic et al. (U.S. Pat. No. 5291607).

Miller et al. and Piosenka et al. teach an apparatus and method that includes the subject matter discussed above. Miller et al. and Piosenka et al. do not mention explicitly that: a microprocessor capable of reading said means for receiving a plurality

of first values and communicating with said means for determining whether an over-temperature condition of said integrated circuit exists; and said microprocessor is capable of writing to said means for receiving a plurality of first values and verifies correct functioning of the controller.

Ristic et al. disclose a microprocessor having environmental sensing capability, and teach that: said microprocessor is capable of reading a plurality of first values representative of the sensed environment, and communicating with means for determining whether an undesirable condition of said environment exists (Fig. 1; col. 3, lines 21-32, lines 40-50 and col. 4, lines 50-63); and said microprocessor is capable of writing to said means for receiving a plurality of first values and verifies correct functioning of the controller (col. 4, lines 50-63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Ristic et al. in the combination of Miller et al. and Piosenka et al. in order to separate the environmental sensing devices from the microprocessor and utilize said microprocessor to process data generated by said sensing devices and in turn allow control of power loads of the environment based on sensed signals (Ristic et al., col. 31-67).

Allowable Subject Matter

11. Claims 7, 8, 14, 15 and 19, 20 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

12. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claims 7, 8, 14 and 15 is the inclusion of the limitation that said temperature measurement buffer is adapted to receive said first value by way of a single wire or a plurality of wires. It is this limitation found in each of the claims, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claim 19 is the inclusion of the limitation of a window size buffer adapted to store a window size value and coupled to said comparator response logic; wherein said comparator response logic operates as an up/down counter, counting said over-temperature conditions and determining whether an over-temperature condition in said integrated circuit exists when said up/down counter reaches said window size value. It is this limitation found in the claim, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 20 is the inclusion of the limitation of a window size buffer adapted to store a window size value and coupled to said comparator response logic; wherein said comparator response logic operates as a counter, counting said over-temperature conditions occurring sequentially and determining whether an over temperature condition in said integrated circuit exists when

said counter reaches said window size value. It is this limitation found in the claim, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 23 is the inclusion of the limitation that said response comprises one of the group of assert an over-temperature pin, assert an over-temperature bit in an error buffer of said controller, assert an over-temperature bit in an error buffer of said microprocessor, issue an over-temperature interrupt to a service bus of said integrated circuit, cause a trap, slow an operating frequency of said integrated circuit, stop said integrated circuit, and do nothing. It is this limitation found in the claim, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes this claim allowable over the prior art.

The primary reason for the allowance of claims 24 and 25 is the inclusion of the limitation of an interface from said response buffer to a microprocessor to enable said microprocessor to write to said response buffer. It is this limitation found in each of the claims, as it is claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

13. Applicant's arguments with respect to claims 1-6, 9-13, 16, 17, 21, 22, 26-38 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-6, 9-13, 16, 17, 21, 22, 26-38 are rejected as new art (U.S. Pat. No. 5406630 to Piosenka et al.) has been found to teach a controller for monitoring die temperatures of an integrated circuit, including a comparator response logic coupled to comparators for determining in response to a comparison of a first value to a second value by said comparators whether an over-temperature condition in an integrated circuit exists. Detailed responses are given in sections 2-9 set forth above in this Office Action.

Contact Information

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

XS
March 29, 2004

John Barlow
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